

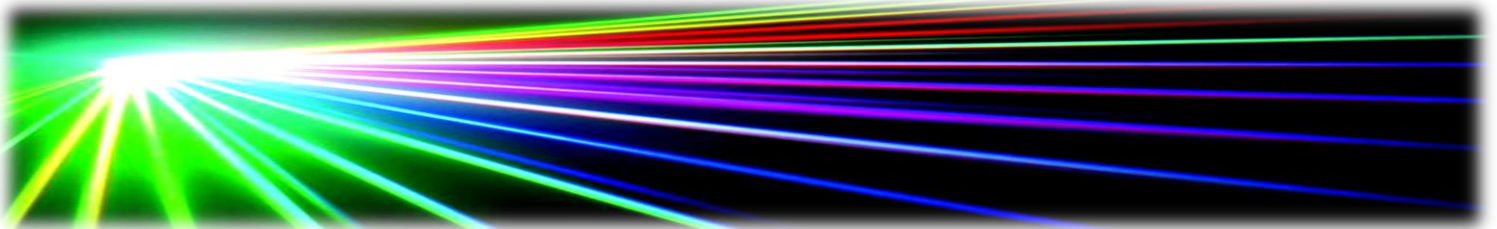
**Harvatek Surface Mount CHIP LEDs Data Sheet**  
**Q3413RGB**  
**(Preliminary)**

**Function and Features:**

- Serial communication with ISELED® compliance.
- Bi directional, half-duplex, 2MBit/s, serial communication.
- Pre-Calibrated Individual R.G.B LED to specified intensity.
- Pre-Calibrated Blue & True Green LED color to 2nm range.
- Brightness & color stability over temperature.
- 8 bit brightness resolution for red, green, and blue LED.
- Temperature compensation on red for constant brightness.
- Build-in diagnostic functions.
- Auto addressing of LED via the serial bus in daisy chain.
- Environmental friendly, RoHS compliance.

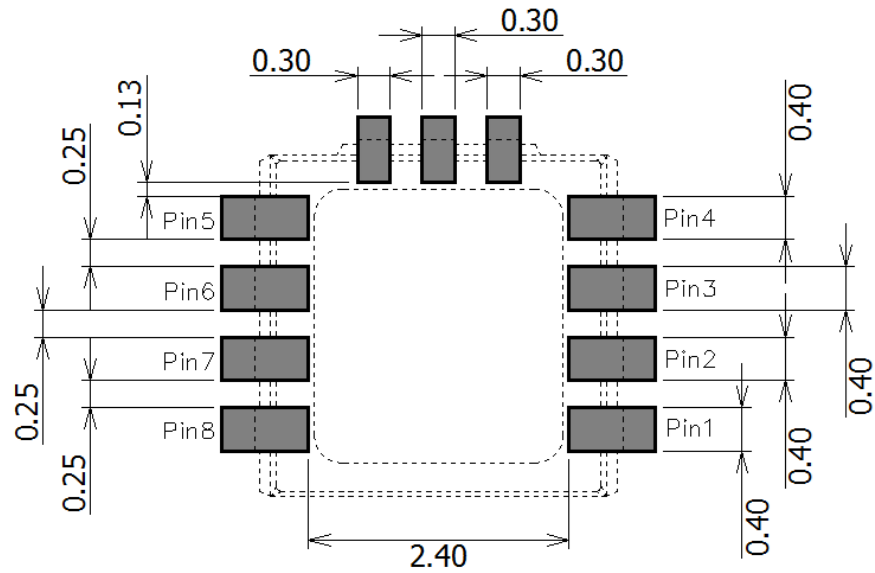
**Applications**

- Automotive interior & exterior lighting.
- Backlight.



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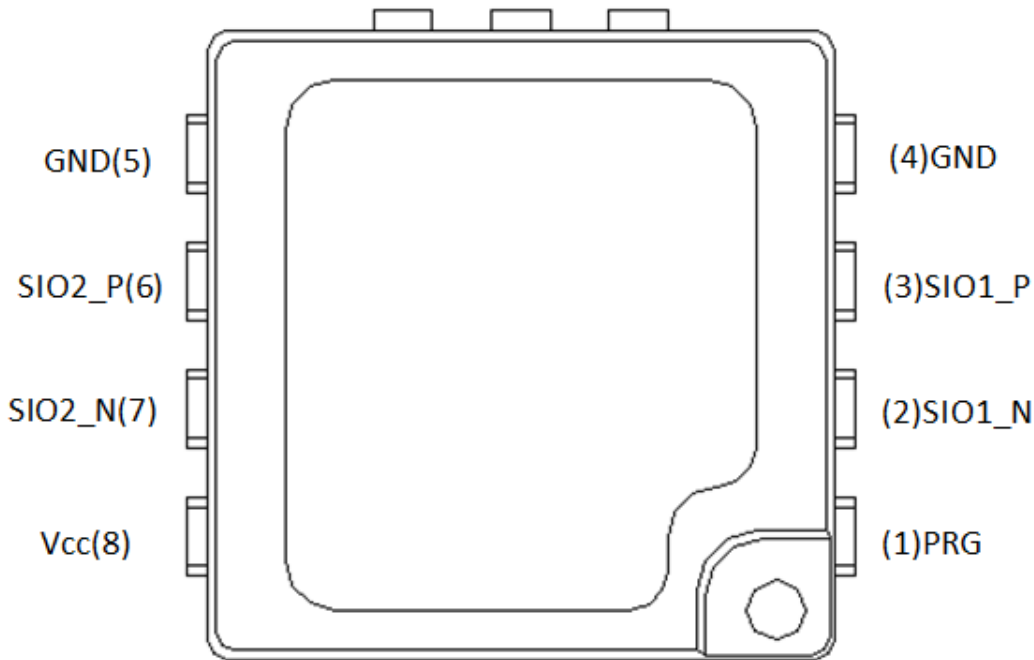




TOP View

Soldering terminals may shift in the x, y direction.

## Pad Description



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Pin Number	Pin Name	Descriptio
1	PRG	Has to be connected to GND for proper operation
2	SIO1_N	Serial Communication Interface Master Side, Negative Polarity
3	SIO1_P	Serial Communication Interface Master Side, Positive Polarity
4/5	GND	Ground
6	SIO2_P	Serial Communication Interface Slave Side, Positive Polarity
7	SIO2_N	Serial Communication Interface Slave Side, Negative Polarity
8	VCC	5V Supply Voltage

## Recommended Operating Conditions

Parameter	Min	Typ.	Max.	Unit
VCC Voltage	4.5	5.0	5.5	V
V SIO1_PV SIO1_N (Serial IO Voltage)	4.5	5.0	5.5	V

## Serial Interface

Parameter	Description	Min.	Typ.	Max.	Units
$f_{SIO1\_P, \text{single ended}}$	Single ended data rate SIO1_P	1.4	2	2.6	MHz
$f_{SIO1\_N, \text{single ended}}$	Single ended clock rate SIO1_N	2.8	4	5.2	MHz
$V_{IH, se}$	Single ended input high voltage	1.20	-	-	V
$V_{IL, se}$	Single ended input low voltage	-	-	1.14	V
$V_{IAmp, diff}$	Differential input amplitude	150	250	325	mV
$V_{OAmpl, diff}$	Differential output amplitude	175	250	325	mV

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## Supply Current

Parameter	Descr	Min.	Max.	Units
LED Green	Peak current	0	80	mA
LED Blue	Peak current	0	80	mA
LED Red	$I_{avg} = I_{peak}$	0	25	mA
Driver	Stand by	0.9	1.1	mA

## Power-On-Reset (POR)

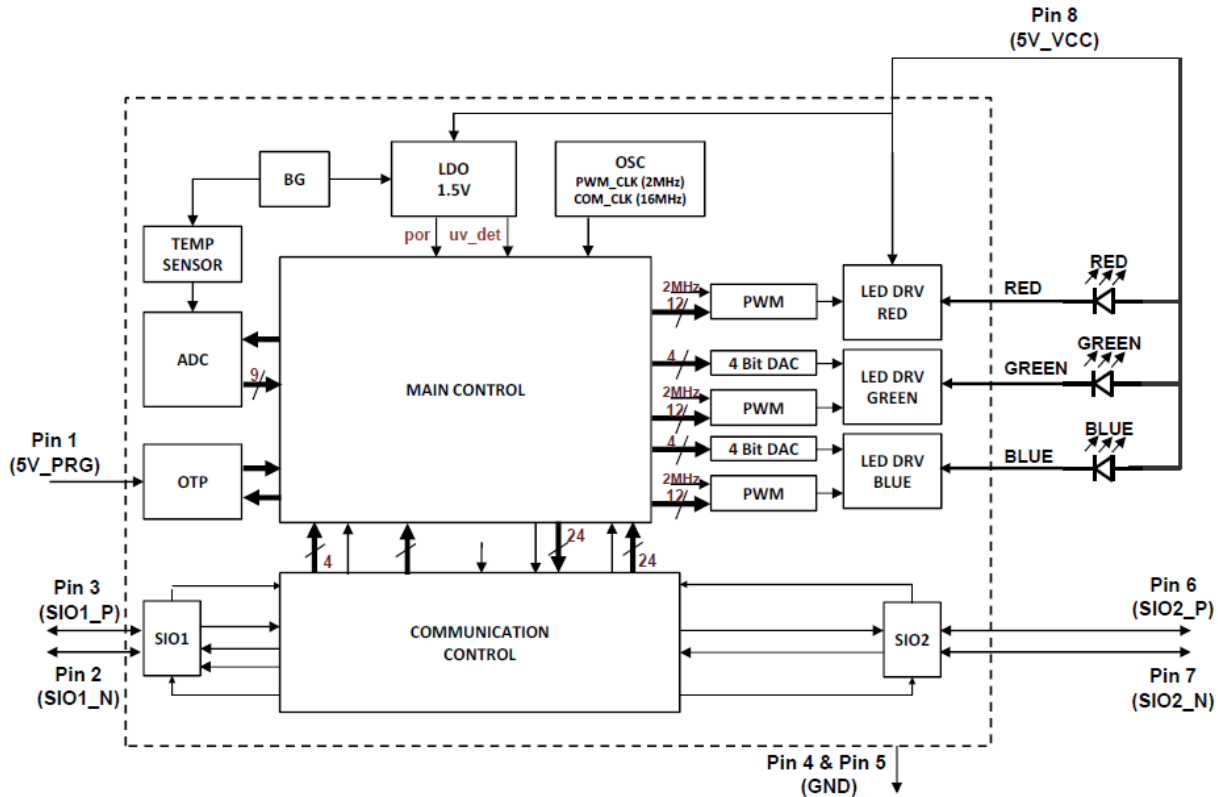
Parameter	Min.	Typ.	Max.	Units
$V_{POR}$	4.0	4.2	4.4	V

## Under voltage-lockout

Parameter	Min.	Typ.	Max.	Units
$V_{uvlo}$	3.2	3.3	3.4	V

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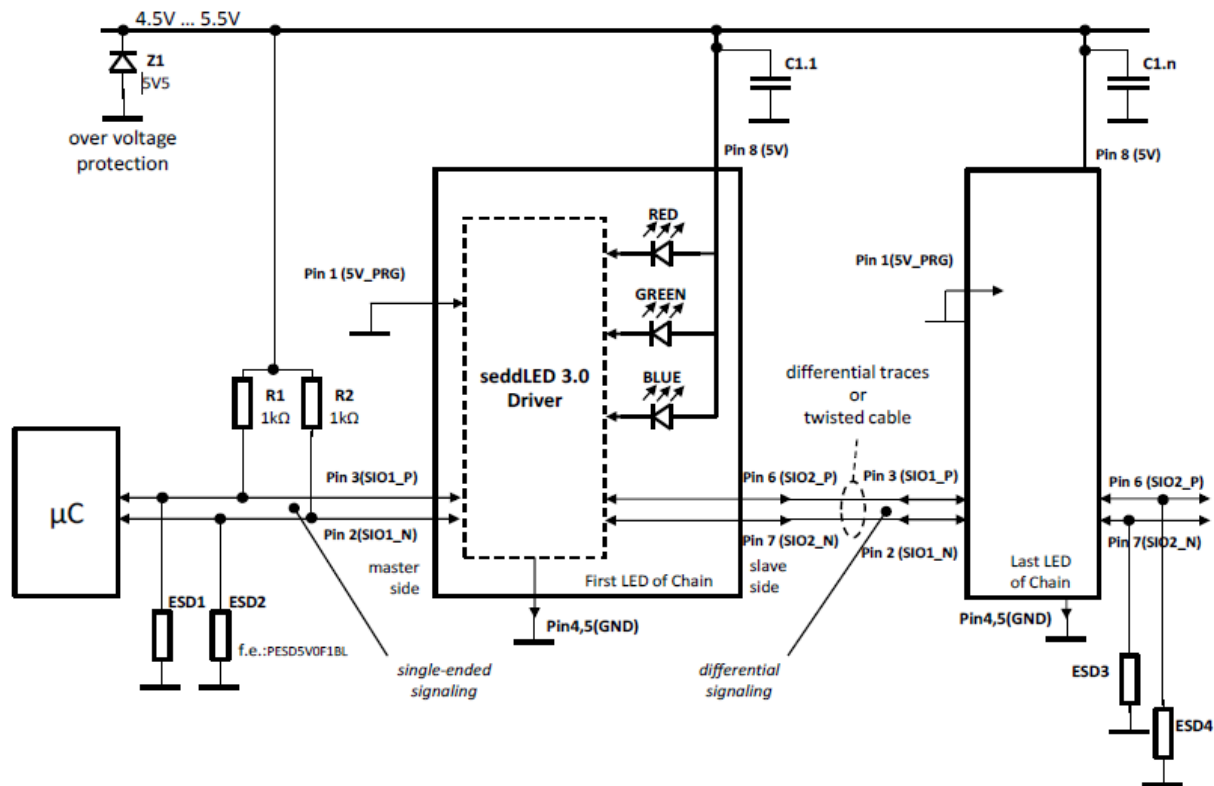
**Functional Block Diagram**



The device implements a communication for the reception of control commands and for providing device status and configuration data. Low side, configurable constant current sinks are provided for controlling 3 LEDs (RGB). The Main Unit computes the PWM duty cycles from the incoming commands and applies the corresponding control values to the three PWM units. The Main Unit is also in charge of a periodic temperature measurement and an appropriate duty cycle adjustment for the red PWM channel. The actual device temperature is obtained via an integrated analog-digital converter (ADC). Besides the temperature the ADC can also measure various other analog values. These measurements are always triggered by a command from the host. The result of the corresponding A/D conversion is also retrieved by a host command. As each device is individually calibrated to compensate for production variations, the corresponding parameters can be stored in an on-die non-volatile memory. This one-time-programmable memory (OTP) is read at hardware reset and the parameters are copied from the OTP to directly accessible registers.

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## Typical Application Layout

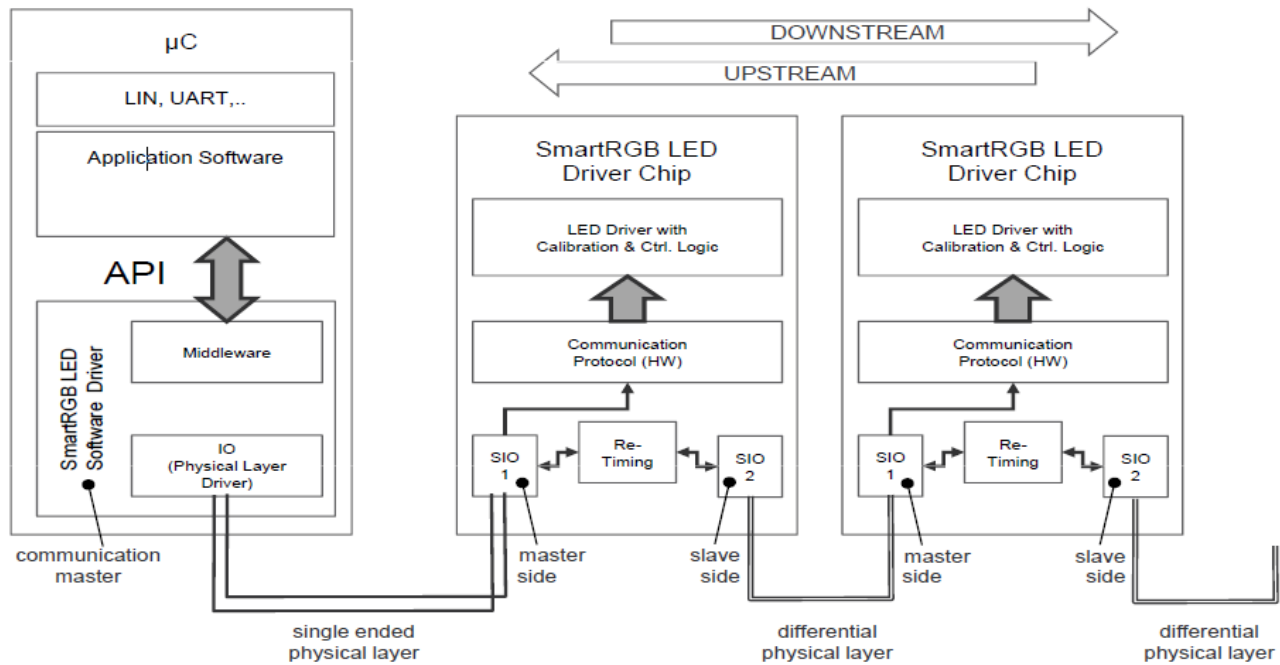


In order to prevent voltage drops, it is recommended to mount the capacitors C1 closely to the  $V_{CC}$  pin. The dimensioning of the capacitors depends on the PCB layout and the supply concept.

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## Functional Description

### Serial Communication



The attachment to the adjacent devices in the chain is made up by two bidirectional differential serial communication lines. The direction towards the controlling microcontroller device is referred to as the “upstream” connection. The opposite direction towards the end of the chain is the “downstream” link. Both links are controlled by the communication unit. Incoming command frames from upstream and responses from downstream are passed to the main unit which is responsible for command processing and overall device control. Commands always originate from the controlling microcontroller. The microcontroller is referred to as the “host” in this document.

The gross data rate on the serial line is 2Mbit/s, i.e. each bit has a nominal duration of 500 ns. As the on-die oscillator has a very limited accuracy, the actual bit time may vary significantly. The whole system is designed for a maximum oscillator variance of  $\pm 30\%$ . With the nominal oscillator frequency being 16 MHz, the actual frequency range is 11.2-20.8MHz.

The device directly attached to the host does not use the differential line mode on the upstream side. Instead a single-ended line mode is used. The single-ended mode is intended to allow for

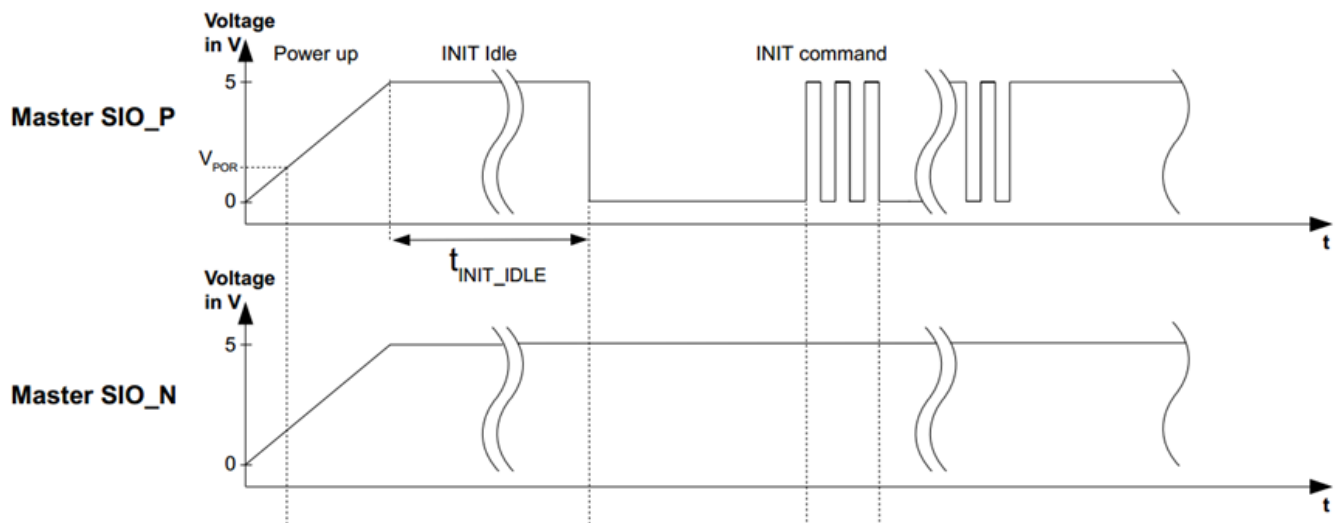
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an easy attachment to industry standard microcontrollers. Both single-ended lines require an external pull-up at the microcontroller to 5V.

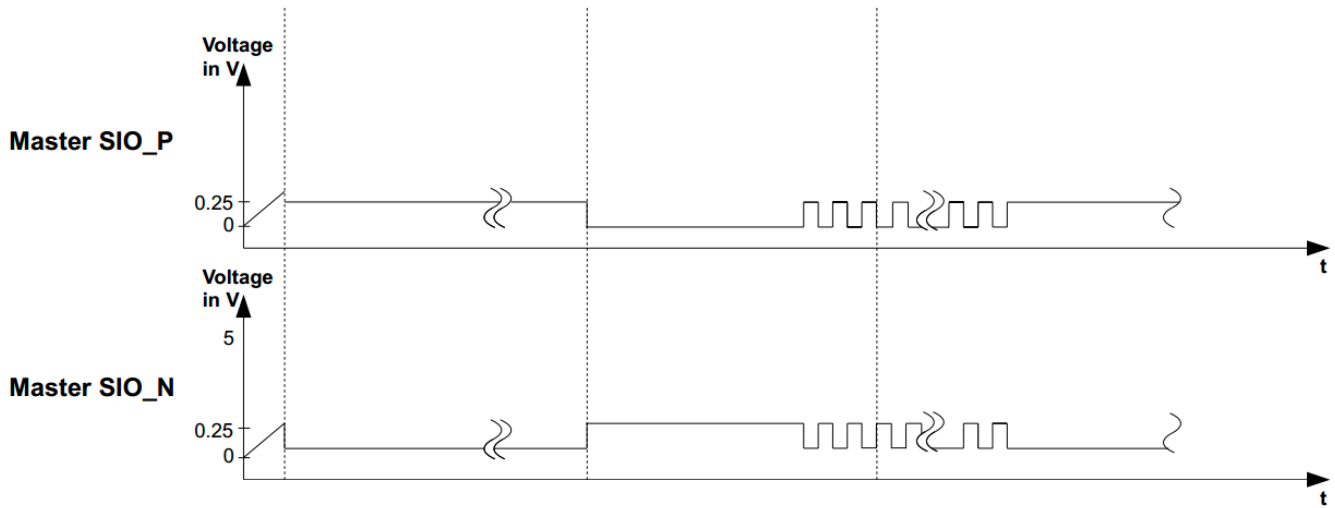
**Automatic Detection of the Serial Line Mode**

During start-up, the devices automatically detect the mode of the upstream and the downstream link. The upstream link may be either single-ended or differential. If a device detects the upstream to be single-ended, it is the first in the chain of LEDs. The downstream link may be either differential or unconnected, i.e. the device is the last in the chain of LEDs. After power-up, an idle of  $t_{INIT\_IDLE} = 150\mu s$  is recommended before the initialization. If during the initialization, while receiving the enumeration command, the master SIO\_N pin is single ended high (5V), the device is switched into single ended communication mode for this port. The detected mode is stored and used for all following communications until a power cycle or a reset command.



Single ended startup (first device in chain)

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Differential startup (devices in chain >1)

Parameter	Description	Min.	Units
t <sub>INIT Idle</sub>	INIT Idle directly after power up	150	μs

### Half-Duplex Communication

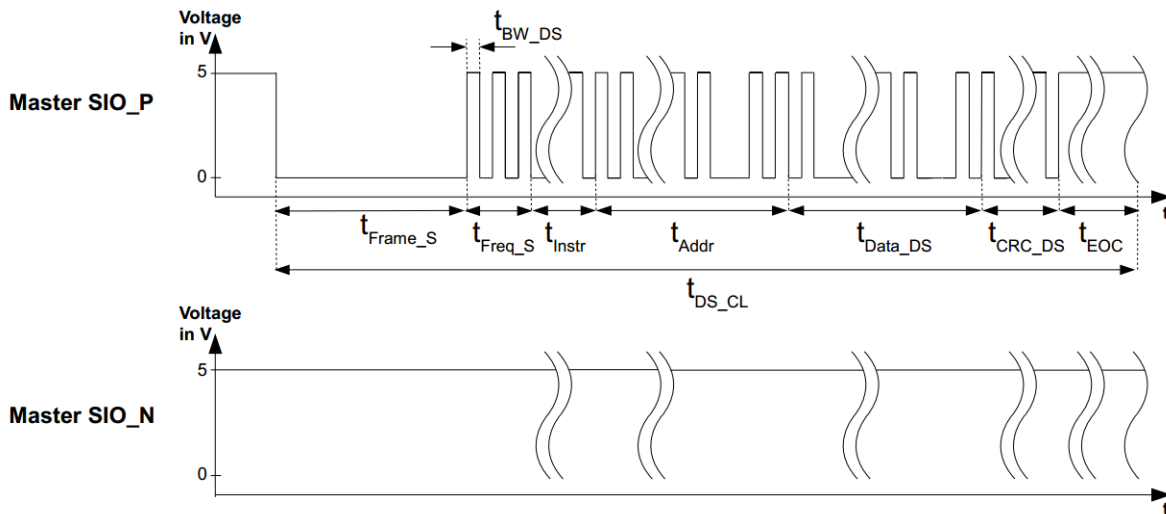
The communication operates in a strict master slave manner. I.e. the microcontroller as the master always initiates a communication. Depending on the type of command the LED devices may send a response (read access) or just silently execute the command (write access). There are three basic types of commands which are described in the following.

### Basic Frame Format

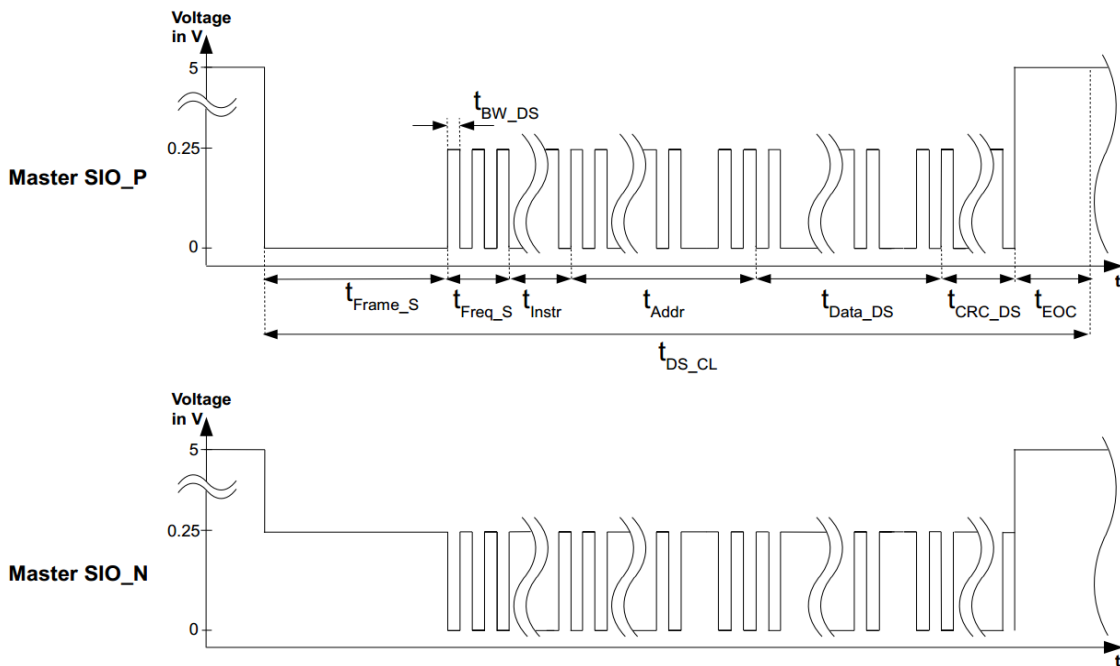
Commands and the response to commands are transmitted with serial frames. A serial frame always consist of a frame\_sync section, followed by a frequency\_sync section, followed by a run length coded command section and finally terminated with an optional CRC section. The command and the CRC sections differ in length between downstream and upstream frames. The chosen bit encoding ensures a maximum number of adjacent zeros of 4 and a maximum number of adjacent ones of 5 on the serial line. Some of the bit patterns which cannot occur during regular data transmission are used for special purposes. A pattern of 6 or more 1-bits is considered as the bus-idle condition. The bus is idle, when no communication is currently ongoing. A pattern of 15 0-bits is recognized as the so-called frame synchronization. This is the sequence to begin a new frame. The pattern “10101” is the so-called frequency synchronization

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pattern. It is used after the frame synchronization to determine the transmitter's gross data rate. Downstream communication is defined as data inputs at SIO1 and outputs at SIO2. This is the data flow for write commands. Upstream respectively is defined as data inputs at SIO2 and outputs at SIO1. This is the data flow for the read response.



Single ended downstream command frame

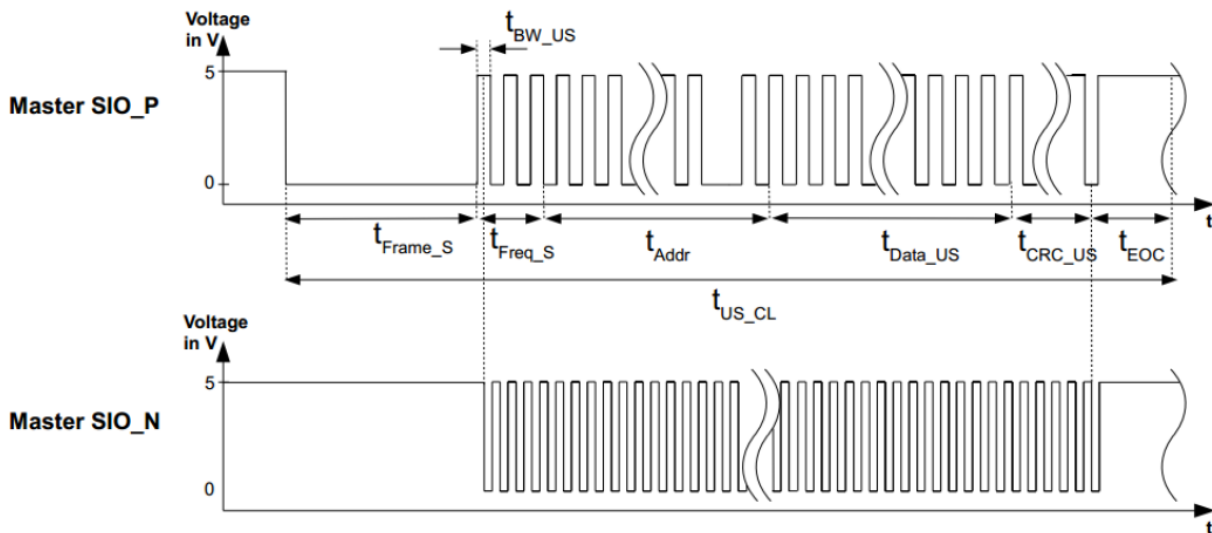


Differential downstream command frame

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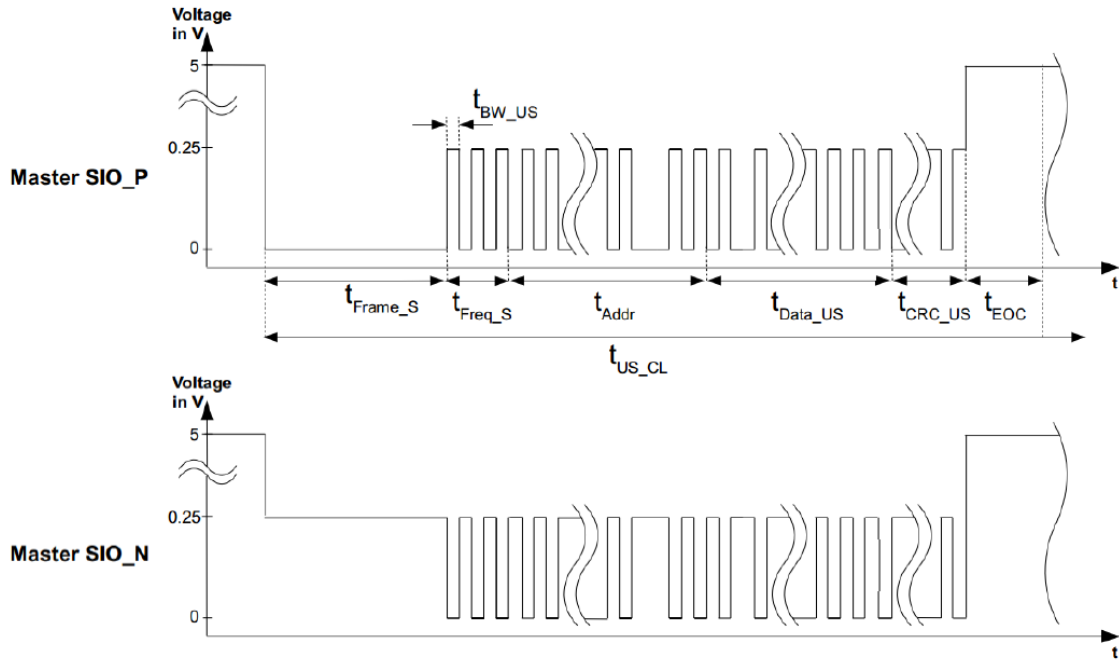
## Downstream command frame parameters

Parameter	Description	Min.	Typ.	Max.	Units
$t_{BW\_DS}$	Downstream bit width	384	500	714	ns
$t_{DS\_CL}$	Downstream command length	CRC enabled		$86 \times t_{BW\_DS}$	
		CRC disabled		$76 \times t_{BW\_DS}$	
$t_{Frame\_S}$	Frame sync		$15 \times t_{BW\_DS}$		
$t_{Freq\_S}$	Frequency sync		$5 \times t_{BW\_DS}$		
$t_{Inst}$	Instruction		$5 \times t_{BW\_DS}$		
$t_{Addr}$	Address		$15 \times t_{BW\_DS}$		
$t_{Data\_DS}$	Downstream data		$30 \times t_{BW\_DS}$		
$t_{CRC\_DS}$	CRC downstream		$10 \times t_{BW\_DS}$		
$t_{EOC}$	End of command idle		$6 \times t_{BW\_DS}$		



Single ended upstream response frame

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Differential upstream response frame

## Upstream command frame parameters

Parameter	Description	Min.	Typ.	Max.	Units
$t_{BW\_US}$	Upstream bit width	384	500	714	ns
$t_{US\_CL}$	Upstream command length	CRC enabled	$61 \times t_{BW\_US}$		
		CRC disabled	$56 \times t_{BW\_US}$		
$t_{Frame\_S}$	Frame sync		$15 \times t_{BW\_US}$		
$t_{Freq\_S}$	Frequency sync		$5 \times t_{BW\_US}$		
$t_{Addr}$	Address		$15 \times t_{BW\_US}$		
$t_{Data\_US}$	Upstream data		$15 \times t_{BW\_US}$		
$t_{CRC\_US}$	CRC upstream		$5 \times t_{BW\_US}$		
$t_{EOC}$	End of command idle		$6 \times t_{BW\_US}$		

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**Bit Retransmission**

To ensure a correct bit-timing, the forwarded data is regenerated with the clock of the device. The retransmission starts with its own frame-sync when it can be guaranteed that a valid frame-sync timing can be created. A new frequency synchronization is only created after the freq-sync on the reception side has been received (the first four bits). Therefore, the minimum propagation delay tpd introduced by the retransmission is four bit widths t<sub>BW</sub>.

Name	Description	Min.	Typ.	Max.	Unit
tpd	Propagation delay	2	4	5.2	μs

To guarantee a correct bit-timing the device uses its own clock as reference and will never transmit faster than its own bit-timing defines, but if the received freq-sync was slower, this timing is used for the retransmission.

The retransmission uses a FIFO to compensate for speed differences between reception and transmission.

Due to the variance in the oscillator clocks of different devices, after each transmission a pause of 30% of the nominal transmission time has to be introduced.

**Initialization**

The digLED\_Init\_Strip command initializes a particular ISELED chain by issuing the command on an associated ISELED communication channel.

This command is always the first command to be transmitted after power-up or reset. The command initializes a chain of devices by assigning the address of the device and by enabling or disabling the phaseshift, the CRC and temperature compensation functions. The digLED\_Init\_Strip command is always executed with a CRC checksum. This is true for both, the command and the response frame.

If any command is received by a device before initialization, the command is always considered as illegal and the error status bit for an undefined command is set. This may happen in the chain's first device only, as a non-initialized device does not forward received messages.

If the first device in the chain receives a digLED\_Init\_Strip command, it takes the received address as its own device address and afterwards transmits another digLED\_Init\_Strip frame to

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the next device in the chain. It increments the address before the transmission. As the adjacent devices proceed in the same manner, the devices in the chain get enumerated with ascending addresses. When the final device in the chain recognizes there is no receiving device at its downstream link, it transmits a response frame upstream. The response frame to a digLED\_Init\_Strip command carries the configuration word read from the OTP. It also transmits the own devices address just initialized.

All upstream devices wait for the responses to be received and forward them towards the microcontroller.

If a frame with an address equal to the adjacent device address (own address plus one) is received, the own response to the digLED\_Init\_Strip command is transmitted thereafter. If the first device has transmitted its response frame, the chain is ready to process regular commands (non-Init frames).

As soon as a device is initialized, it unconditionally forwards incoming correct frames (Frame-Sync, Freq-Sync and the RLC coding as well as the frame length are checked) to the adjacent node in the chain.

Frames received from upstream are forwarded downstream and vice versa. If an error is detected, the forwarding is stopped for this frame.

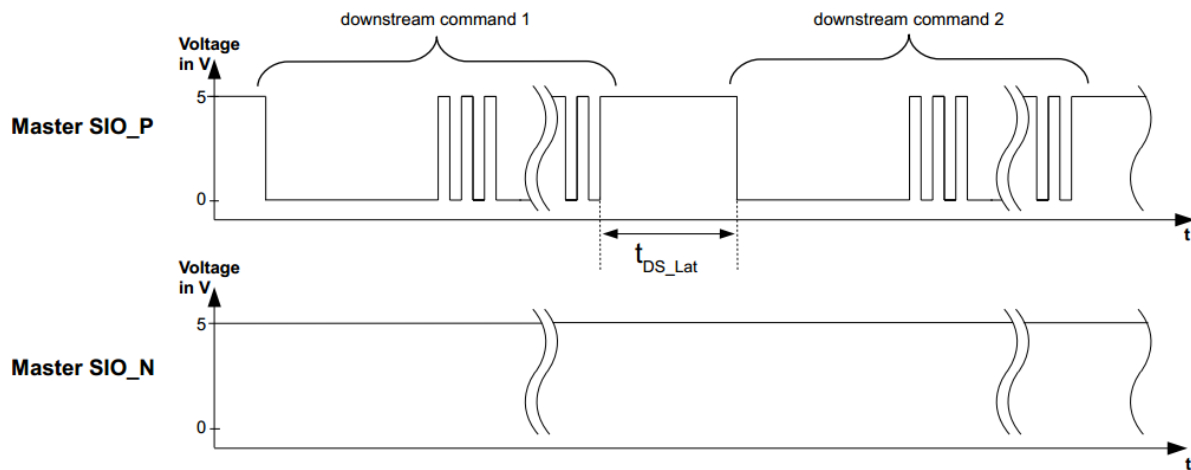
Name	Description	Equation
t <sub>INIT</sub>	Initialization duration	n X (t <sub>DS_CL</sub> + t <sub>US_CL</sub> + 2 X t <sub>PD</sub> )

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**Write Access**

Most commands of the LED Controller are write-only commands. I.e. the devices receive a command frame and execute the appropriate actions without any further communication. A write access command may be directed to a single device (unicast), to all devices(broadcast), or to a defined group of devices (multicast).

As every command frame is forwarded downstream irrespective of its destination address, all stations always receive all commands. Only its execution depends on the commands destination address. To avoid communication issues, it is recommended to wait 30% of the command length between two consecutive commands.



Multiple single ended downstream commands

Parameter	Description	Min.
$t_{DS\_Lat}$	Latency between two downstream commands	$0.3 \times t_{DS\_CL}$

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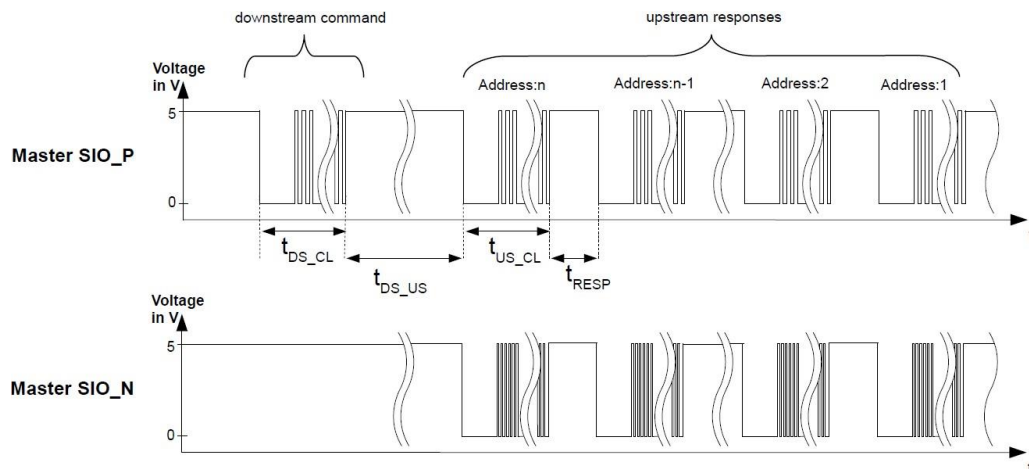
### Read Access

A read access consists of two phases, the command and the response phase. The command phase uses downstream communication and the response phase uses upstream communication. Commands for read access do not use the command address, i.e. these commands may not be directed to a device based on the device address.

There are two commands for read access, digLED\_Read and digLED\_Ping. The digLED\_Read commands retrieve a status information from all devices and the digLED\_Ping command is used to check the device chain’s integrity. Only the final node in the chain responds to a PING command.

A digLED\_Read command is first received by all devices via the frame in downstream direction. The last node in the chain then immediately transmits its response frame upstream. The response frame’s data field depends on the actual digLED\_Read command. The response frame’s address field is set according to the own device’s address. All the nodes upstream forward all received response frames until a frame with the address of their adjacent node is received. Then the respective node transmits its own response frame. This procedure lasts until the chain’s first node has transmitted its response frame.

A digLED\_Ping command is similar to a digLED\_Read command, but only the last device in the chain responds to a digLED\_Ping. Thus, the digLED\_Ping command is executed much faster than a regular digLED\_Read command.



**Single ended read command and responses**

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Name	Description	Equation
t <sub>DS_US</sub>	Delay between down- and upstream	t <sub>DS_CL</sub> + t <sub>US_CL</sub> + 2 x n x t <sub>PD</sub>
t <sub>RESP</sub>	Delay between responses	0.3 x t <sub>US_CL</sub>

**Down- and upstream delay, delay between responses**

## Timeouts

The digLED\_Init\_Strip, all the digLED\_Read, and the digLED\_Ping commands initiate upstream data transmission. With the digLED\_Init\_Strip and the read commands all nodes are expected to send a response to the host. The digLED\_Ping requires only the last node in the LED chain to respond. However, in all cases each node needs to await all responses originating from the nodes downstream. Thereafter either the node's own response is transmitted or new commands are accepted. Only the last node in the LED chain may immediately transmit its response.

In case there is an error with the chain downstream, not all expected responses may arrive. Thus, each of the commands expecting a response waits for a certain time only and then returns to its previous state without having transmitted the node's response data.

The lengths of the timeouts depend on the respective command. They are calculated to account for the worst-case oscillator frequency tolerance. I.e. the waiting node has a high-speed clock and all the nodes waited for have a low speed clock. The hardware implementation uses an internally divided clock for the timeout counter:

$$f_{[timeout]} = f_{[osc]} / 214$$

With the nominal clock frequency of 16MHz the counter's resolution results to 1.024ms.

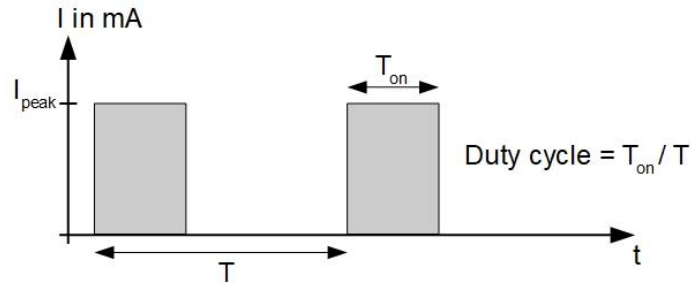
Command	Max. counter value	Min. timeout	Nom. timeout	Max. timeout	Units
digLED_Init_Strip	992	780.6	1015.3	1451.2	ms
digLED_Read_*	427	335.6	436.7	624.6	ms
digLED_Ping	62	48.0	63.0	90.7	ms

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## PWM Units

### Basic Mode of Operation

The LED controller device incorporates three independent PWM channels, one for each LED.



**PWM Signal**

The resolution is 12 bit. The supported duty cycles are 0/4095 to 4095/4095. The nominal PWM output frequency is  $16\text{MHz}/215 = 488.3\text{Hz}$ . The frequency is reduced to the half or the quarter of this frequency with low duty cycles. This ensures a minimum on-time of  $2\mu\text{s}$  for the LEDs. The minimum output frequency is 122Hz. The output frequency is not derived from the actual PWM duty cycle but from the RGB value received from the host. As the DIM command also has impact to the LED intensity, it is accounted for as well. The actual relationship is given in the following table

### DIM parameter relationships between RGB parameters and PWM frequencies

DIM	RGB	PWM Frequency			Unit
		Min.	Typ.	Max.	
0	8 ... 255	341.6	488	634.4	Hz
	4 ... 7	170.8	244	317.2	Hz
	0 ... 3	85.4	122	158.6	Hz
1	16 ... 255	341.6	488	634.4	Hz
	8 ... 15	170.8	244	317.2	Hz
	0 ... 7	85.4	122	158.6	Hz
	32 ... 255	341.6	488	634.4	Hz
	16 ... 31	170.8	244	317.2	Hz

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2	0 ... 15	85.4	122	158.6	Hz
	64 ... 255	341.6	488	634.4	Hz
3	32 ... 63	170.8	244	317.2	Hz
	0 ... 31	85.4	122	158.6	Hz

## Update

When a new PWM duty cycle has to be applied, this is always done at the end of a PWM cycle. I.e. the PWM always completes an output cycle using the previously active duty cycle and starts the next output cycle using the updated duty cycle.

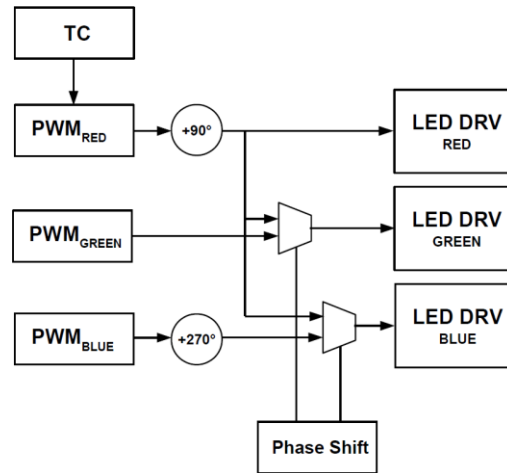
## Phase Shift

To spread the LED's current consumption over time, the three PWM channels have a fixed phase shift to each other. This phase shift is retained even if the output frequency of the channels is different. If a channel is operating at a lower frequency, it may be considered to leave out one or three full PWM cycles. When leaving power save mode, the channels are restarted appropriately to again obtain the correct phase shift.

The fixed phase shift is defined in the following table. Please note the absolute phase shift times are nominal values. I.e. they are subject to vary with the internal oscillator's frequency.

PWM Channel	Rel. Phase Shift	Unit	Abs. Phase Shift
Green	0	%	0
Red	25	%	0.25 / PWM Frequency
Blue	75	%	0.75 / PWM Frequency

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**Power Save Mode**

When all LED channels are set to an intensity of 0, the device enters a power save mode for the current sources driving the LEDs. I.e. the digLED\_Set\_RGB command must be issued with an RGB value of 0x000000 to enter the power save mode.

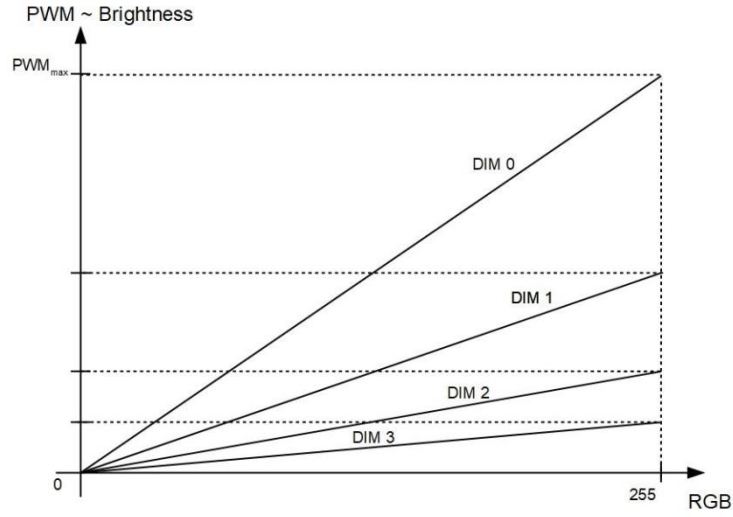
Recovering from this mode does not require any particular measures. I.e. the host just needs to issue a digLED\_Set\_RGB command with the data field different from 0x000000 and the current sources are restarted again. There is a delay of approx. 1µs before the restart of the green PWM channel (no phase shift applies to the green channel).

This is due to an internal ramp-up required by the analog circuitry. The same procedure is applied after device power-up or a hardware reset, as the initial RGB value is 0x000000. I.e. the LEDs are all turned off after power-up or a hardware reset.

**DIM Function for Accurate Low Light Colors**

To extend the digLED\_Set\_RGB command’s resolution for accurate low light colors, the seddLED provides the digLED\_Dim command. The command divides the PWM duty cycles computed from the RGB setting. There are four divisors available. Details are shown in below Figure and Table.

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## DIM Functio

DIM	Relative PWM Ratio
0	1
1	1/2
2	1/4
3	1/8

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